IN THE CLAIMS

Claims 31, 33, and 35 have been amended. A clean copy of the pending claims, as amended, is provided below. Amended claims are indicated so. A marked-up version of the amended claims follows the clean copy.

CLEAN COPY OF PENDING CLAIMS

1 31. (Three Times Amended) A memory device, comprising:

2 a memory array;

3 a register to store at least one bit indicating a suspend status of a write operation

4 for the memory array; and

5 a control circuit coupled to said memory array and said register, said control

6 circuit to update said register and to control an output of a status signal representing said

7 suspend status of said write operation, and wherein said control circuit includes:

8 a first state machine to receive commands for accessing said memory

9 array or said register, and

10 a second state machine coupled to said first state machine and to execute

11 the commands received by said first state machine.

1 32. (Unchanged) The memory device of claim 31, wherein said write operation

2 represents a byte write operation.

1 33. (Amended) The memory device of claim 31, wherein said status signal

2 represents a byte write suspend command.

2

1   34.   (Unchanged)   The memory device of claim 31, wherein said control circuit is to

2   receive a status request signal and said register is to output said status signal in response

3   to said status request signal, said status signal having a first state to indicate said write

4   operation is suspended and a second state to indicate said write operation is not

5   suspended.

1   35.   (Amended)   The memory device of claim 31, further comprising:

2   at least one data input/output coupled to said control circuit, wherein the at least

3   one data input/output is to receive said status request signal from a processor and to

4   provide said status signal to said processor.

1   36.   (Unchanged)   The memory device of claim 31, further comprising:

2   a status output coupled to said register, wherein said status output is to provide a

3   second status signal if said status output is polled, and wherein said second status signal

4   having a first state to indicate said write operation is suspended and a second state to

5   indicate said write operation is not suspended.

1   37.   (Unchanged)   The memory device of claim 31, wherein said status request signal

2   is a read status register command.

3